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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/416,368	10/12/1999	DAVID J. CORISIS	3770.2US-(97	6085

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JOSEPH A WALKOWSKI
TRASK BRITT & ROSSA
P O BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/416,368	CORISIS ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 18-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 18-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *30 May 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The proposed drawing correction filed on 5-30-3 has been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations of the embodiments of claims 1 and 23, "a lead frame having a plurality of conductors and at least one alignment feature electrically isolated from the plurality of conductors," "removing the at least one alignment feature," and, "coupling at least some of the plurality of conductors to a semiconductor die," the limitations of the embodiment of claim 23, "coupling the at least one alignment feature with a portion of a testing device; testing the integrated circuit package through at least some of the electrically coupled conductors; decoupling the at least one alignment feature from the portion of the testing device," and the features of the embodiment of claim 21, must be shown or the features canceled from the claims. To continue to afford applicant the benefit of compact prosecution, it is noted that the present illustrations of some of these individual limitations do not show every feature of the invention specified

in the claims because the illustrations are drawn to embodiments other than the embodiments of claims 1, 21 and 23. Further, the proposed drawing corrections filed on 5-30-3 do not show every feature of the embodiments of claims 1, 21 and 23. For example, (not exhaustive) proposed Figure 9 does not show "at least one alignment feature electrically isolated from the plurality of conductors."

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3, 4 and 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato (5728601).

At column 4, line 29 to column 8, line 31, column 11, lines 14-39, and column 12, lines 14-20, Sato teaches the following:

3. A method of forming an integrated circuit package, the method comprising: providing a plurality of conductors 24 and at least one alignment feature 23b; coupling 27 at least some of the plurality of conductors to a semiconductor die 25; and encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material 21.

4. A method of forming and testing an integrated circuit package, the method comprising: providing a plurality of conductors and at least one alignment feature; electrically coupling at least some of the plurality of conductors to a semiconductor die; encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device ["conductor pattern provided on the substrate that may be a printed circuit board"]; and testing the integrated circuit package through at least some of the electrically coupled conductors.

24. The method according to claim 3, further comprising forming the at least one alignment feature to include an alignment cut-out.

25. The method according to claim 3, further comprising coupling a heat spreader 22 to the external surface [not labeled] of the insulating material, forming at least one other alignment feature "the engaging portion of the support member" in the heat spreader.

26. The method according to claim 3, further comprising providing a tie bar 23a and forming the at least one alignment feature in the tie bar.

To further clarify the teaching of testing the integrated circuit package through at least some of the electrically coupled conductors, it is noted that it is inherent in the process of electrically coupling the conductors to the circuit board and attempting to operate the package, that the package is put to a test of operability; it must operate (and to some degree of operability) or fail to operate, therefore, it is inherently tested.

To further clarify the teaching of coupling the heat spreader 22 to the external surface of the insulating material, it is noted that Sato teaches coupling the heat spreader 22 to the external surface of the insulating material by fastening

together and linking the heat spreader 22, at least indirectly, to the external surface of the insulating material.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

In the alternative, claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sato as applied to claim 4 supra, and further in combination with King (6420195).

Because Sato does not appear to literally teach coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and testing the integrated circuit package through at least some of the electrically coupled conductors, in the alternative, claim 4 is rejected over the combination of Sato and King.

At column 1, line 62 to column 7, line 65, King teaches coupling at least one alignment feature 50 encompassed by insulating material 46 with a portion 58 of a testing device 56; and testing an integrated circuit package 40 through at least some electrically coupled conductors 44. Moreover, it would have been obvious to combine the process of King with the process of Sato because it would enable package testing and improve manufacturing quality.

Claims 3, 4 and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by King (6420195).

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not

the invention "by another," or by an appropriate showing under 37 CFR 1.131.

At column 4, line 25 to column 5, lines 26, column 6, lines 29-38, and column 7, line 41 to column 8, line 35, King teaches the following:

3. A method of forming an integrated circuit package, the method comprising: providing a plurality of conductors 44 and at least one alignment feature 50; coupling at least some of the plurality of conductors to a semiconductor die 42; and encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material 46.

4. A method of forming and testing an integrated circuit package, the method comprising: providing a plurality of conductors and at least one alignment feature; electrically coupling at least some of the plurality of conductors to a semiconductor die; encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device 56; and testing the integrated circuit package through at least some of the electrically coupled conductors.

24. The method according to claim 3, further comprising forming the at least one alignment feature to include an alignment cut-out.

Claims 1, 18-21 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Solstad (4689875).

At column 3, line 15 to column 5, line 49, Solstad teaches the following:

1. A method of forming an integrated circuit package, the method comprising: forming a lead frame 10 having a plurality of conductors 16A, 16B and at least one alignment feature 12A electrically isolated from the plurality of conductors; coupling at least some of the plurality of conductors to a semiconductor die 20; encapsulating the semiconductor die and a portion of the lead frame with an insulating material 26, 32; and removing the at least one alignment feature subsequent the encapsulating the semiconductor die and a portion of the lead frame.

18. The method according to claim 1, further comprising forming the at least one alignment feature to include at least one aperture.

19. The method according to claim 1, further comprising forming the at least one alignment feature to include a plurality of apertures 12A, 12B.

20. The method according to claim 1, further comprising forming a separation line 22A in the lead frame and wherein removing the at least one alignment feature further comprises removing the at least one alignment feature along the separation line.

21. The method according to claim 20, wherein the forming a separation line in the lead frame includes perforating [between the conductors] the separation line.

23. A method of forming and testing an integrated circuit package, the method comprising: forming a lead frame having a plurality of conductors and at least one alignment feature electrically isolated from the plurality of conductors; coupling at least some of the plurality of conductors to a semiconductor die; encapsulating the semiconductor die and a portion of the lead frame with an insulating material; coupling the at least one alignment feature with a portion of a testing device ["testing station" including 40A]; testing the integrated circuit package through at least some of the electrically coupled conductors; decoupling the at least one alignment feature from the portion of the testing device; and removing the at least one alignment feature subsequent the decoupling the at least one alignment feature from the portion of the testing device.

To further clarify the teaching of coupling the alignment feature with a portion of a testing device, as cited, Solstad teaches that alignment feature 12A is a socket provided for driving the lead frame along a path from "station to station for processing." Further, Solstad teaches that the lead frame is passed under the testing station for testing. Therefore, it is inherent that the alignment feature is coupled to the driving portion of the testing device.

Claims 1 and 18-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Geist (4961107).

At column 3, line 17 to column 4, line 12, column 5, line 63 to column 6, line 15, and column 7, lines 14-24, Geist teaches the following:

1. A method of forming an integrated circuit package, the method comprising: forming a lead frame 10 having a plurality of conductors 20 and at least one alignment feature 12 electrically isolated from the plurality of conductors; coupling at least some of the plurality of conductors to a semiconductor die 26; encapsulating the semiconductor die and a portion of the lead frame with an insulating material 36; and removing the at least one alignment feature subsequent the encapsulating the semiconductor die and a portion of the lead frame.

18. The method according to claim 1, further comprising forming the at least one alignment feature to include at least one aperture 28.

19. The method according to claim 1, further comprising forming the at least one alignment feature to include a plurality of apertures.

20. The method according to claim 1, further comprising forming a separation line [longitudinal edge of 32 illustrated but not labeled] in the lead frame and wherein removing the at least one alignment feature further comprises removing the at least one alignment feature along the separation line.

21. The method according to claim 20, wherein the forming a separation line in the lead frame includes perforating the separation line [between "supports 24"].

22. The method according to claim 1, further comprising forming the at least one alignment feature to include a tab 12.

Applicant's amendment and remarks filed 5-30-3 have been fully considered, are addressed by the rejection supra, and are further addressed infra.

Applicant's arguments directed to the rejections of claims 1 and 18-23 under 35 U.S.C. 112, first paragraph are deemed persuasive and the rejections are withdrawn.

Also, applicant contends that Sato does not teach substantially encompassing the at least one alignment feature with an insulating material.

This contention is respectfully traversed because, as cited, for example, in Figure 6(C), Sato teaches substantially encompassing the at least one alignment feature with an insulating material by substantially forming a circle 21x about the alignment feature 23b with an insulating material 21.

In addition, applicant alleges, "one of ordinary skill in the art would clearly not modify Sato so as to substantially encompass the lead frame cutouts 23b with insulating material as such a configuration would likely reduce, if not eliminate, the quality of any electrical connection between the lead frame cutouts 23b and the support legs 22 and thereby impair any grounding function effected by such a connection."

This allegation is respectfully traversed because, at column 6, lines 9-12, Sato teaches that the ground connection is optional. Furthermore, the allegation is unsupported by proof or a showing of facts; hence, it essentially amounts to mere conjecture. Ex parte Gray, 10 USPQ2d 1922 (Bd. Pat. App. & Inter. 1989) (statement in publication dismissing the "preliminary identification of a human b - NGF - like molecule" in the prior art, even if considered to be an expert opinion,

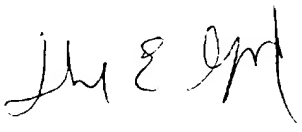
was inadequate to overcome the rejection based on that prior art because there was no factual evidence supporting the statement); In re Beattie, 974 F.2d 1309, 24 USPQ2d 1040 (Fed. Cir. 1992) (declarations of seven persons skilled in the art offering opinion evidence praising the merits of the claimed invention were found to have little value because of a lack of factual support); Ex parte George, 21 USPQ2d 1058 (Bd. Pat. App. & Inter. 1991) (conclusory statements that results were "unexpected," unsupported by objective factual evidence, were considered but were not found to be of substantial evidentiary value).

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 703-306-3329.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/3087724.



David E. Graybill
Primary Examiner

Art Unit 2827

D.G.
5-Aug-03